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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/737,119	12/17/2003	Hiroshi Kuroda	XA-10006	5995

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EXAMINER	
NGUYEN, DILINH P	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/737,119	KURODA ET AL.	
	Examiner	Art Unit	
	DiLinh Nguyen	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 6-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1-3 and 10-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Katagiri et al. (U.S. Pat. 6841881) (newly cited).

Katagiri et al. disclose a semiconductor device comprising:

a wiring substrate 1;

a microcomputer chip 2C (fig. 2, column 9, line 62); and

a memory chip 2A or 2B (fig. 2, column 7, line 47), the microcomputer chip and the memory chip being mounted over an upper surface of the wiring substrate, and

wherein the microcomputer chip is constructed as a multiport device including an interface between the microcomputer chip and another part of the system including the memory chip and an interference between the microcomputer chip and outside of the system,

wherein the memory chip is constructed to be accessed from the outside of the system via the microcomputer chip,

wherein the microcomputer chip 2C has a substantially square planar shape (fig. 33),

wherein the memory chip 2A has a substantially rectangular planar shape, with a long side having a greater length than a side thereof adjacent to the long side (fig. 33),

wherein a length of a side of the microcomputer chip 2C is shorter than a length of a long side of the memory chip 2A (fig. 33), and

wherein the microcomputer chip 2C is mounted over the wiring substrate in as state being stacked over the memory chip such that the microcomputer chip covers a portion of the long side of the memory chip and covers no portion of the side of the memory chip adjacent to the long side (figs. 2 and 33).

- Regarding claim 2, Katagiri et al. discloses that the microcomputer chip 2C is connected to first electrodes 9 of said wiring substrate via a plurality of bonding wires 8, the memory chip 2A is connected to second electrodes of said wiring substrate via a plurality of bump electrodes 4, said first electrodes are arranged toward an outer periphery side of said wiring substrate from the second electrodes (fig. 2).
- Regarding claim 3, Katagiri et al. disclose that the memory chip includes a flash memory (column 7, line 47).
- Regarding claim 10, Katagiri et al. disclose that the microcomputer chip and the memory chip have respective terminals, a number of terminals of the microcomputer chip being much greater than a number of terminals of the memory chip (figs. 2 and 33).

- Regarding claim 11, Katagiri et al. disclose that the terminals of the memory chip 2A or 2B are arranged such that they are not superposed over the terminals of the microcomputer chip in a plan view (fig. 2 and 33).

3. Claims 1-3 and 10-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Kado et al. (U.S. Pat. 7042073) (newly cited).

Kado et al. disclose a semiconductor device comprising:

a wiring substrate 1;

a microcomputer chip 2C (cover fig., abstract); and

a memory chip 2A or 2B (cover fig., abstract), the microcomputer chip and the memory chip being mounted over an upper surface of the wiring substrate, and

wherein the microcomputer chip is constructed as a multiport device including an interface between the microcomputer chip and another part of the system including the memory chip and an interference between the microcomputer chip and outside of the system,

wherein the memory chip is constructed to be accessed from the outside of the system via the microcomputer chip,

wherein the microcomputer chip 2C has a substantially square planar shape (fig. 17),

wherein the memory chip 2A has a substantially rectangular planar shape, with a long side having a greater length than a side thereof adjacent to the long side (fig. 17),

wherein a length of a side of the microcomputer chip 2C is shorter than a length of a long side of the memory chip 2A (fig. 17), and

wherein the microcomputer chip 2C is mounted over the wiring substrate in as state being stacked over the memory chip such that the microcomputer chip covers a portion of the long side of the memory chip and covers no portion of the side of the memory chip adjacent to the long side (cover fig. and fig. 17).

- Regarding claim 2, Kado et al. discloses that the microcomputer chip 2C is connected to first electrodes 9 of said wiring substrate via a plurality of bonding wires 8, the memory chip 2A or 2B is connected to second electrodes of said wiring substrate via a plurality of bump electrodes 4, said first electrodes are arranged toward an outer periphery side of said wiring substrate from the second electrodes (cover fig.).
- Regarding claim 3, Kado et al. disclose that the memory chip includes a flash memory (cover fig., abstract).
- Regarding claim 10, Kado et al. disclose that the microcomputer chip and the memory chip have respective terminals, a number of terminals of the microcomputer chip being much greater than a number of terminals of the memory chip (fig. 17).
- Regarding claim 11, Kado et al. disclose that the terminals of the memory chip 2A or 2B are arranged such that they are not superposed over the terminals of the microcomputer chip in a plan view (cover fig. and fig. 17).

4. Claims 1-3 and 6-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hiroaki et al. (JP. 2001-291821) (previously applied) in view of Kanemoto et al.

(U.S. Pat. 6410987) (previously applied) and further in view of Goller et al. (U.S. Pat. 6683374) (newly cited).

- Regarding claims 1 and 6, Hiroaki et al. disclose a semiconductor device comprising:

a wiring substrate 8;

an upper chip 14; and

a lower chip 10 or 12, the upper chip and the lower chip being mounted over an upper surface of the wiring substrate, and

wherein the upper chip is constructed as a multiport device including an interface between the upper chip and another part of the system including the lower chip and an interference between the upper chip and outside of the system,

wherein the lower chip is constructed to be accessed from the outside of the system via the upper chip,

wherein the upper chip 14 has a substantially square planar shape,

wherein the lower chip 10 or 12 has a substantially rectangular planar shape, with a long side having a greater length than a side thereof adjacent to the long side,

wherein a length of a side of the upper chip 14 is shorter than a length of a long side of the lower chip, and

wherein the upper chip 14 is mounted over the wiring substrate 8 in as state being stacked over the lower chip 10 or 12 (fig. 1, abstract).

Hiroaki et al. do not explicitly disclose the upper chip and lower chips are the microcomputer chip or the memory chip such that the microcomputer chip covers a

portion of the long side of the memory chip and covers no portion of the side of the memory chip adjacent to the long side.

However, Kanemoto et al. disclose a semiconductor device comprising: a square ASIC (microcomputer) chip 2 is stacked over a rectangular flash memory chip 3 (fig. 5, column 9, lines 33-42) in order to select the flash memory chip or the microcomputer chip in the chips of Hiroaki et al. because it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

Goller et al. disclose a semiconductor device comprising : a chip 2 has a substantially square planar shape; a chip 1 has a substantially square planar shape; wherein the chip 1 has a substantially rectangular planar shape with a long side having a greater length than a side thereof adjacent to the long side, wherein a length of a side of the chip 1 is shorter than a length of the long side of the chip 1 such that the chip 2 cover a portion of the long side of the chip 1 and covers no portion of the side of the chip 1 adjacent to the long side (figs. 3 and 5), in order to provide a semiconductor package structure with reliably connected electrically to one another in a small space (fig. 5).

Therefore, it would have been obvious to one having ordinary in the art at the time the invention was made to select the flash memory chip or the microcomputer chip in the chips of Hiroaki et al. and the microcomputer chip covers a portion of the long side of the memory chip and covers no portion of the side of the memory chip adjacent

to the long side as taught by Goller et al. in to the device of Hiroaki et al. because it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex Parte Masham, 2 USPQ F.2d 1647 (1987) and in order to provide a semiconductor package structure with reliably connected electrically to one another in a small space.

- Regarding claim 2, Hiroaki et al. discloses that the upper chip 14 is connected to first electrodes of said wiring substrate 8 via a plurality of bonding wires 19, the lower chip 10 or 12 is connected to second electrodes of said wiring substrate 8 via a plurality of bonding wires 17, said first electrodes are arranged toward an outer periphery side of said wiring substrate from the second electrodes (fig. 1).
- Regarding claim 3, Kanemoto et al. disclose that the memory chip includes a flash memory (fig. 5, column 9, lines 36-37).
- Regarding claim 7, Hiroaki et al. disclose that the upper chip 14 is connected to first electrode of the wiring substrate 8 via a plurality of bonding wires 19, a lower chip 10 of the two chips is connected to second electrodes of the wiring substrate 8 via a plurality of bumps electrodes 9, the chip 12 is connected to third electrodes of the wiring substrate 8 via a plurality of bonding wires 17, the first electrodes are arranged toward an outer periphery of the wiring substrate from the second and third electrodes (fig. 1, abstract).
- Regarding claim 8, Kanemoto et al. disclose a semiconductor device comprising

the memory chip includes a flash memory (fig. 5, column 9, lines 36-37) and it would have been obvious to one having ordinary skill in the art to form the lower chip 10 or 12 of Hiroaki et al. includes DRAM.

- Regarding claim 9, Hiroaki et al. disclose a lower surface of the wiring substrate 8 is formed with a plurality of bump electrodes 22 constructing external connection terminals (fig. 1).

- Regarding claim 10, Hiroaki et al. disclose the upper chip 14 and the lower chips 10 or 12 have respective terminals, and it would have been obvious to form a number of terminals of the upper chip being much greater than a number of terminals of the lower chips (fig. 1). Moreover, the number of terminals would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the number of terminals giving unexpected results, it is not inventive to discover number by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen number or upon another variable recited in a claim, the Applicant must show that the chosen number is critical. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed, Cir. 1990).

- Regarding claim 11, Hiroaki et al. disclose the terminals of the lower chips 10 or 12 are arranged such that they are not superposed over the terminals of the upper chip 14 in plan view (fig. 1).

- Regarding claim 12, Hiroaki et al. disclose that an under fill resin 21 is filled in a

gap between the lower chip 10 and the wiring substrate 8 (fig. 1).

Response to Arguments

Applicant's arguments with respect to claims 1-3 and 6-12 have been considered but are moot in view of the new ground(s) of rejection. See the new grounds of rejection above.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DLN

HOAI PHAM
PRIMARY EXAMINER